

DEC STD 140-1 Documentation Requirements for Printed-Wiring Boards (50-Class)

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ABSTRACT: This section of DEC STD 140 defines the minimum documentation structure required for the release of 50-class printed-wiring boards. DEC STD 140-0 Documentation, Data, and Release Requirements for Printed-Wiring Boards, Modules, and Backplanes — Introduction provides an introduction and general requirements for the standard.

APPLICABILITY: The documentation requirements defined in this standard are mandatory for all 50-class boards, 54-class modules, and 70-class/option backplanes released by Digital.

STATUS: APPROVED 27-Sep-1991; use VTX SMC for current status.

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1 INTRODUCTION

This section of DEC STD 140 defines the standard documentation structure and the contents of the printed-wiring board (PWB) documentation packages required for the release of 50-class PWBs.

2 PWB (50-CLASS) DRAWING DIRECTORY REQUIREMENTS

Drawing Directories (DDs) are the controlling documents for PWB drawings and serve as an index to the PWB documentation package.

The purpose of the 50-class DD is to allow 50-class packages to be ECOed separately from 54-class packages, and to treat the PWB as a separate part. Refer to *DEC STD 185-0 Documentation of Computer Media in the Engineering Documentation System* for information on PC data requirements.

The structure and content of the PWB document package are summarized in Table 1. All documents listed in Table 1 shall be included on 50-class DD. The document identification system is defined in *DEC STD 012-1 Documentation Identification Conventions Including Mnemonic Codes*. The part revision system is defined in *DEC STD 012-0 Part Identification Standard*.

The Circuit Drill and Etch Mechanical Detail (MD) and PC Data or Index are mandatory and shall be listed on the 50-class drawing directory.

DEC STD 024 Top Document Requirements (all sections) provides a description of the specific content requirements for drawing directories.

Table 1: Printed-Wiring Board (50-Class) Documentation Base

Drawing Type	Drawing Number Format
Drawing Directory (for a PWB)	B-DD-50XXXXX-X-X
Circuit Drill and Etch Mechanical Detail (MD)	D-MD-50XXXXX-X-X
Soldermask Drawing, as required	
Nonstandard Circuit Drawing, as required	
Nomenclature, as required	
PC Data or Index	K-PC-50XXXXX-X-DB or K-IF-50XXXXX-X-DB

NOTE

There is no longer a separate etch cut drawing. This information is now provided as part of the Unit Assembly (UA). Refer to *DEC STD 140-2 Documentation Requirements for 54-Class Modules and Backplanes*.

3 CIRCUIT DRILL AND ETCH MECHANICAL DETAIL — DRAWING FORMAT AND CONTENT REQUIREMENTS (50-CLASS)

The purpose of the Circuit Drill and Etch Mechanical Detail (MD) drawing is to define in detail the mechanical features of the circuit design. The MD shall contain references to any additional drawings and specifications needed to support PWB fabrication.

3.1 DRAWING FORMAT REQUIREMENTS

Refer to EL-EN400-00 through EL-EN416-00 Special Feature Drawing Formats in EL-ENPCB-00, *PC Board Engineering Handbook—Special Feature Drawings* for basic drawing format requirements. All drawings that use computer media as a master must use a document identifier that meets the requirements of DEC STD 185-0.

3.2 MINIMUM DATA BLOCK REQUIREMENTS

The following subheads explain the preferred method for entering data on an MD. Unique requirements should be worked with the DEC STD 140 Committee or waived. Use an *X* to indicate appropriate choices or enter the required data.

3.2.1 Tolerance Block

The Tolerance block, shown in Figure 1, defines general tolerances to be used when a specific tolerance is not listed on the drawing, or the tolerance may be included in a separate specification referenced by a note. Refer to *DEC STD 114-1 Engineering Drawing Requirements—Dimensioning and Tolerancing for Engineering Drawings*.

NOTE

These tolerances are not in agreement with those shown in *DEC STD 013-1 Standard Engineering Drawing Formats and Forms—General Purpose Drawing Sizes and Formats*, but are specific to printed-wiring boards. Metric designs require metric tolerances.

Figure 1: Tolerance Block

TOLERANCES		
INCHES UNLESS OTHERWISE SPECIFIED		
INCHES	mm	ANGLES
.XXX ± .010	,XX ± .25	± 0 DEG
.XX ± .020	,X ± .50	30 MIN
.X ± .100	X, ± 2.50	

3.2.2 Title/Approval Block

All approval blocks must be completed before document release. Figures 2 and 3 show sheet 1 and the continuation sheet of the Title/Approval block.

The Title/Approval block shall contain the names of the following responsible individuals and the date of approval:

- **DRAWN** — Name of responsible PC layout designer
- **CHECKED** — Name of responsible PC layout checker
- **MECH ENG** — Name of engineer responsible for the mechanical integrity of the product
- **PROJ ENG** — Name of design engineer responsible for the product design

- **MFG ENG** — Name of the responsible site producibility engineer

The following information is also required in the Title/Approval block. The continuation sheet shall contain identical information as required. See Figure 3.

- **SCALE** — Enter 1:1. The circuit image shown on the MD shall be 1:1.
- **SHEET _____ OF _____** — Enter the sheet number and total number of sheets used.
- **TOP DOC NO** — Enter the number of the top document shown on the 50-class DD, if applicable.
- **TITLE** — Enter *CIRCUIT DRILL AND ETCH DRAWING*.
- **SIZE** — Enter the drawing size.
- **CODE** — Enter *MD* for the 50-class mechanical drawing (three locations on MD format).
- **NUMBER** — Enter the assigned 2-5-2 50-class part number (three locations on MD format).
- **REV** — Enter the current document revision (three locations on MD format). See heading 3.
- **ETCH REV** — Enter the current etch revision. See heading 5.1.
- **MEDIA** — Enter *K* for electronic media and *D* for paper media (three locations on MD format).

Figure 2: Title/Approval Block, Sheet 1

APPROVALS	DATE
DRAWN:	
CHECKED:	
MECH ENG:	
PROJ ENG:	
MFG ENG:	
SCALE:	
SHEET 1 OF	
TOP DOC NO:	

digital ™			
TITLE:			
SIZE	CODE	NUMBER	REV
ETCH REV:			MEDIA

Figure 3: Title/Approval Block, Continuation Sheet

TITLE	DOCUMENT NUMBER			
	SIZE	CODE	NUMBER	REV
	SCALE		SHEET	OF

3.2.3 Copyright Block

Refer to *DEC STD 128-0 Security Classifications for Engineering Intellectual Property—Policy and Regulations* for the contents of the Copyright block.

3.2.4 Sample Revision Block

The Revision block, shown in Figure 4, shall contain the following information in the appropriate column and shall not be completed at initial release.

- **DATE** — Date the ECO is signed-off.
- **RESPONSIBLE ENGINEER** — First initial and last name of the responsible engineer.
- **ECO NUMBER** — Refer to EL-EN100-1A, *Engineering ECO Coordination Procedure*.
- **REV** — The current document revision.

Figure 4: Revision Block

DATE	RESPONSIBLE ENGINEER	ECO NUMBER	REV

When the documentation is redrawn, as in the case of a relayout, the revision block and the Title/Approval block shall be completed with new names and dates. Refer to subhead 3.2.2 for further information.

3.2.5 Hole Data Block

The Hole Data block, shown in Figure 5, shall contain the following information in the appropriate block:

- **SYMBOL** — Indicate the symbol used to locate proportionately positioned hole locations. A separate symbol must be used for each different finished hole size.
- **FINISHED HOLE SIZE** — Indicate finished hole size with dimensions consistent with the requirements of subhead 3.3.1.
- **POSITIVE TOLERANCE** — Indicate positive tolerances if other than those required by *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*. Refer to subhead 3.3.1.
- **NEGATIVE TOLERANCE** — Indicate negative tolerances if other than those required by DEC STD 176-0. Refer to subhead 3.3.1.
- **PLATED ?** — Indicate *Y* if plated-through holes or *N* if nonplated-through holes. Plated and nonplated holes of the same size are not allowed.
- **QUANTITY** — Indicate the number of occurrences of hole sizes for each symbol.
- **FROM LAYER** _____ **TO LAYER** _____ (applies to all boards including boards with buried vias (BVs)).

Figure 5: Example of Completed Hole Data Block (inches)

HOLE DATA (FOR STANDARD HOLE TOLERANCES USE DEC STD 176)						
SYMBOL	+	⋈	⊥	⧲	⊚	
FINISHED HOLE SIZE (INCHES)	0.020	0.032	0.038	0.070	0.129	
POSITIVE TOLERANCE (INCHES)		0.003				
NEGATIVE TOLERANCE (INCHES)		0.000				
FINISHED HOLE SIZE (mm)						
POSITIVE TOLERANCE (mm)						
NEGATIVE TOLERANCE (mm)						
PLATED ?	Y	Y	Y	Y	Y	
QUANTITY	190	16	100	16	32	
FROM LAYER <u>1</u> TO <u>4</u>						

3.2.6 Design Information Block

The Design Information block is shown in Figure 6. Use an *X* to indicate choices. The following information is required:

- **NUMBER OF LAYERS** — Indicate the number of conductive layers.
If using a layer construction found in EL-ENPCB-00, reference the appropriate drawing directory in the *LAYER CONSTRUCTION* field. If using another specification for the layer construction, check *AS SHOWN* and either reference it here or provide layer construction information on the MD.

- **CONTROLLED IMPEDANCE** — Indicate whether controlled impedance and/or controlled capacitance will be used.
- **SURFACE MOUNT TECH/MINIMUM PITCH** — Indicate which side(s) contain surface mount footprints by entering the minimum pitch of the SMT pads. If none, enter *NONE* for that side.
- **PLANAR RESISTOR TECHNOLOGY** — Indicate whether planar resistor technology will be used. Check *NO* if PRT is not used. Otherwise check *YES* and indicate the number of PRT layers. The number of PRT layers does not affect the overall layer count.
- **BOARD FINISH** — Indicate whether tin lead, hot air solder level (HASL), all copper, or some other finish will be used.
- **SOLDERMASK** — Indicate where soldermask will be used.
 - Indicate on which side(s) soldermask is required. Check *NONE* or *SIDE 1* and/or *SIDE 2*.
 - Indicate if soldermask over bare copper (SMOBC) is used. Check *YES* or *NO*.
- **NOMENCLATURE** — Indicate on which side(s) nomenclature is required. Check *NONE* or *SIDE 1* and/or *SIDE 2*.
- **TENTED VIAS** — Indicate if vias are tented. Check *YES* or *NO*.

When using tented vias, dry film requirements must be added in the MD notes.

- **MINIMUM VIA HOLE SIZE:** — Indicate the minimum via hole size.
- **PAD EXPANSION** —
 - Check *OUTER LAYERS*, if pad expansion is used on outer layers.
 - Check *SIGNAL INNER LAYERS*, if used on signal inner layers.
 - If pad expansion is not used, check *NONE*.

If pad expansion is not allowed due to electrical restrictions, leave this field blank and specify this in a note. Refer to *DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements* for design requirements.

- **INCIRCUIT THIEVING** —
 - If incircuit thieving is not used, check *NONE*.
 - If incircuit thieving is not part of the engineering data, indicate on which side(s) incircuit thieving is required. Check *SIDE 1* and/or *SIDE 2*.
 - If incircuit thieving is part of the engineering data, check *AS SHOWN*.
 If void areas are required for electrical reasons, check the *SPECIAL REQUIREMENTS* field and create a thieving void table listing the X, Y coordinates of the void outline vertices from H-master 0. See Figure 7.
- **TECHNOLOGY** — Enter the minimum line width (LW) and minimum line spacing (LS) of the board,
- **CIRCUIT OUTLINE/FINGER DETAIL** — If the circuit outline is defined in EL-ENPCB-00, enter the appropriate drawing number. If using a circuit outline not found in EL-ENPCB-00, check *AS SHOWN*. All information for fabrication must be

shown on the MD or in a referenced document or specification. See subhead 3.3.3 for further information.

- **SPECIAL REQUIREMENTS** — Enter any special requirements such as plating,void areas without incircuit thieving, and so on.

Figure 6: Design Information Block

DESIGN INFORMATION	
NUMBER OF LAYERS : _____ LAYER CONSTRUCTION: _____ AS SHOWN: _____	
CONTROLLED IMPEDANCE: YES _____ NO _____ CONTROLLED CAPACITANCE: YES _____ NO _____	
SURFACE MOUNT TECH / MINIMUM PITCH: SIDE 1 _____ SIDE 2 _____	
PLANAR RESISTOR TECHNOLOGY: YES _____ NO _____ NUMBER OF PRT LAYERS _____	
BOARD FINISH: REFLOW TIN LEAD _____ HASL _____ ALL COPPER _____ OTHER _____	
SOLDERMASK: NONE _____ SIDE 1 _____ SIDE 2 _____	SMOBC: YES _____ NO _____
NOMENCLATURE: NONE _____ SIDE 1 _____ SIDE 2 _____	TENTED VIAS: YES _____ NO _____
MINIMUM VIA HOLE SIZE: _____ MINIMUM COMPONENT HOLE SIZE: _____	
PAD EXPANSION: OUTER LAYERS _____ SIGNAL INNER LAYERS _____ NONE _____	
INCIRCUIT THIEVING: NONE _____ SIDE 1 _____ SIDE 2 _____ AS SHOWN _____	
TECHNOLOGY (LW/LS): _____	
CIRCUIT OUTLINE / FINGER DETAIL: _____ AS SHOWN _____	
SPECIAL REQUIREMENTS: _____	

Figure 7: Example of Completed Void Table for Soldermask and Incircuit Thieving

VOID COORDINATES FROM H-MASTER 0				SOLDERMASK	INCIRCUIT THIEVING
VOID	X COORD	Y COORD	SIDE		
1	4.600 5.250 5.250 4.600	9.800 9.800 10.200 10.200	1	X	
2	3.750 4.100 4.100 3.750	8.400 8.400 9.000 9.000	1		X

NOTE

List the X,Y coordinates from H-master 0 of the void outline vertices. The void area must be a polygon with sides parallel to the X and Y axes. Start at the closest corner to H-master 0.

3.2.7 Fabrication Information Block

Pre-Design Producibility may supply manufacturing fabrication information for Design Engineering to complete the drawings, or the information may be included in a separate specification referenced by a note. See Figure 8.

Fabrication information includes:

- **FABRICATE BOARD PER** — A standard assembly board drawing number found in EL-MFPCB-01, *PC Board Manufacturing Handbook - Volume 1* must appear on this line or AS SHOWN must be specified if the board is to be fabricated to the finished circuit size.
- **STEP AND REPEAT CODE** — Indicate the step and repeat code or enter *none*.
- **PRESS FIT COMPONENTS** — Indicate whether press fit components are used.

Figure 8: Fabrication Information Block

FABRICATION INFORMATION		MATERIAL AND WORKMANSHIP FOR ALL FABRICATED PRINTED WIRING BOARDS MUST MEET THE REQUIREMENTS OF DEC STD 176	
FABRICATE BOARD PER:	AS SHOWN	STEP AND REPEAT CODE:	PRESS FIT COMPONENT: YES NO

3.3 MD CONTENT REQUIREMENTS

The MD is the circuit etch and hole drawing and shall include a view showing the circuit outline, hole data, a view of each layer of etch specified on the MD, and soldermask layers if included in the circuit data. Etch views shall be shown from side 1 to the center of the board and the remainder shown from side 2 to the center. Etch views should specify from which side it is viewed. All views may appear on one sheet if the circuit size permits.

Any changes to the PC data shall require a new revision level of the documentation and the PC data base. This includes hole size changes.

Any applicable engineering documents, specifications, control drawings, and/or special requirements shall be listed as a note. Information specified on the MD supersedes all standards and referenced documents.

The preferred notes area is the upper right corner.

3.3.1 System of Dimensioning

The system of dimensioning on the MD shall comply with the requirements of *DEC STD 114-0 Engineering Drawing Requirements—Industry Standards Adopted by Digital Engineering and Manufacturing Documentation Organizations*, DEC STD 114-1, and *DEC STD 015-0 Abbreviations and Units of Measurement*.

When the U.S. Customary (inch) system of dimensioning is used in the PC design data base, the U.S. Customary system of dimensioning shall be used on the MD and all supporting documentation. Dual dimensioning (mm/in) is optional on the MD and all supporting documentation.

When the metric (mm) system of dimensioning is used in the PC design data base, dual dimensioning (mm/in) shall be used on the MD and all supporting documentation. Metric conversions shall be the responsibility of Design.

3.3.2 Mechanical Features

Mechanical features must be dimensioned, and a fabrication datum must be indicated with a defined dimensional relationship to H-master 0 (design data origin point).

3.3.3 Circuit Outlines

Every MD shall have a circuit outline drawn at a 1:1 scale. The circuit outline shall be fully dimensioned as defined in the data, either:

- a. On the MD
- b. On a drawing found in EL-ENPCB-00
or
- c. In a separate specification

If the circuit outline is found in EL-ENPCB-00 or in a separate specification:

- Reference the appropriate drawing or specification number in the *Circuit Outline /Finger Detail* entry of the Design Information block shown in Figure 6.
- Indicate overall length and width as reference dimensions.

Nonstandard circuit outlines not found in EL-ENPCB-00 or in a separate specification shall be shown on the MD with finished circuit size (FCS) dimensions to indicate overall length and width.

New circuit outlines that may be used in future designs may be added to EL-ENPCB-00.

3.3.4 Layer Construction

If a separate layer construction drawing is not referenced, the layer construction information shall be shown on the MD or in a referenced specification.

Nonstandard layer constructions shall be documented with the following information. See Figure 9.

- Layer classification such as signal, power/ground, planar resistor layer, and so on.
- Dielectric minimum thickness shall be specified as a reference for controlled impedance boards only.
- Copper thicknesses (tolerances per A-SP-1400000-GS-0, *Basic Specification for PC Boards and Material, Raw Stock and Finished Goods*)
- Overall thickness and tolerance

Figure 9: Recommended Format for Nonstandard Layer Construction Detail (Dimensions are for example only)

OVERALL DIMENSIONS WITH TOLERANCE	L1 SIG	-----	0.0007 ± 0.0002	INCH
		//////////	0.0046 ± 0.0015	
	L2 SIG	-----	0.0014 ± 0.0002	INCH
		//////////	0.0062 ± 0.001	
	L3 SIG	-----	0.0014 ± 0.0002	INCH
		//////////	0.009 ± 0.002	
	L4 PWR/GND	-----	0.0014 ± 0.0002	INCH
		//////////	0.0065 ± 0.001	
	L5 PWR/GND	-----	0.0014 ± 0.0002	INCH
		//////////	0.009 ± 0.002	
	L6 SIG	-----	0.0014 ± 0.0002	INCH
		//////////	0.0062 ± 0.001	
	L7 SIG	-----	0.0014 ± 0.0002	INCH
		//////////	0.0046 ± 0.0015	
	L8 SIG	-----	0.0007 ± 0.0002	INCH

3.3.5 Soldermask Drawings

Soldermask drawings are required as part of the MD for each layer of soldermask when soldermask is not part of the engineering design data.

When soldermask is part of the engineering design data, it is not necessary to document void areas on the MD.

Soldermask views may be shown in reverse image (negative plot). This shall be noted on the drawing.

Soldermask views shall be shown from the side on which it is applied.

3.3.6 Nomenclature Drawings

Nomenclature drawings are required as part of the MD when nomenclature is required. Nomenclature shall be shown from the side on which it is applied.

3.3.7 Circuit Placement and Dimensioning Features

Circuit placement and dimensioning features are mandatory for MDs. The following requirements apply.

3.3.7.1 Scale

Sheet 1 of the MD shall show the circuit outline at a 1:1 scale, viewed from side 1 (the component side), and shall include proportionately positioned coded hole locations. Overall reference dimensions shall be shown. For further information see DEC STD 140-2.

3.3.7.2 Fabrication Datum

A fabrication datum, marked X and Y is an absolute position from H-master 0 and is the required location for the intersection of the designed right hand and bottom edges of the circuit. The standard location is X2.7 inches, Y1.7 inches from H-master 0.

NOTE

A datum is a fixed reference point and cannot be fabricated. Manufacturing data is located in relation to H-master 0 (the design reference point).

3.3.7.3 First-hole Pickup

A circuit hole (on a 0.025-inch grid to H-master 0), preferably one nearest to the fabrication datum, must be dimensioned from the datum. This will be called the first-hole pickup.

3.3.7.4 Nonplated Holes Larger than 0.250 Inch

All nonplated holes with finished diameters greater than 0.250 inch shall be dimensioned from the datum. See subhead 3.3.7.3.

3.3.7.5 Grandfather Clause

For older circuit designs that do not have the DIGITAL logo and/or a UL frame in the data base, the X,Y coordinate from H-master 0 for that nomenclature must be dimensioned on sheet 1. All new designs shall have the DIGITAL logo and a UL frame in the data base.

3.3.8 Scale

The circuit image shown on the MD shall be created at 1:1. The MD shall specify the drawing size to be plotted.

3.3.9 Vias

When a design requires laminated blind vias (LBVs) or buried vias, a circuit outline drawing and hole outline data table are required for each layer pair or stack. Sheet 1 shall contain a hole data table that is a composite of all holes in the design.

3.3.10 Planar Resistor Technology

When a design requires planar resistor technology (PRT), a separate sheet shall be included in the MD set for each PRT layer that shows the planar resistors viewed from side 1.

A CAD file shall also be provided that defines the following information for each resistor:

- Resistor value expressed in ohms
- Resistor high tolerance expressed as a percent
- Resistor low tolerance expressed as a percent
- Name of the resistor layer
- Reference designator for the resistor under test
- Test point locations for the resistor, (primary and alternate)

3.3.11 Control Characteristics

Control characteristics and their numerical values and test point locations shall be defined on the MD. Control characteristics consist of the electrical parameters of etch DC resistance, characteristic impedance, capacitance, propagation delay, or inductance.

The control characteristics shall be documented with the following information:

Table 2: Documenting Control Characteristics

Comp/Conn Ref Des	Test PT1	Test PT2	Reference Layer	R ohms NOM	L nH NOM	C pF NOM	Z ohms NOM
AAAA	X,Y	X,Y	n	n	n	n	n
BBBB	X,Y	X,Y	n	n	n	n	n
NONE	X,Y	X,Y	n	n	None	n	n

Documentation shall also specify compatible combinations of the following, as shown in Table 3.

- Layers
- Related line widths
- Impedance (ohms)
- DC resistance

Documentation for controlled impedance designs shall also specify the material dielectric constant, for example:

Material dielectric constant = 4.6 at 30 MHz nominal

Table 3: Documentation Requirements for Controlled Impedance Designs

Layer	Nominal Line Width (in)	Zo (ohms)	Maximum DC Resistance (ohms)
L2,L5,L6,L9	0.011 nom.	50 ± 5	0.362 max.

Table 3 (Cont.): Documentation Requirements for Controlled Impedance Designs

Layer	Nominal Line Width (in)	Zo (ohms)	Maximum DC Resistance (ohms)
L1,L10	0.020 nom.	60 ± 5	0.169 max.
L2,L5,L6,L9	0.008 nom.	60 ± 5	0.531 max.
L1,L10	0.012 nom.	75 ± 7	0.313 max.
L2,L5,L6,L9	0.005 nom.	75 ± 7	0.998 max.

3.3.12 Special Testing

If test point locations for special test requirements, such as HIPOT, are not part of the design data base, then those locations shall be identified on the MD or in a separate specification referenced in a note.

Impedance/propagation delay can be tested at special coupons or at internal etch locations. Coupon design or internal test point configurations shall be noted/referenced on the MD to ensure proper impedance probe construction and use.

HIPOT test points shall be documented with the following information. See Figure 10.

Figure 10: HIPOT Test Coordinates

POWER	
X COORDINATE	Y COORDINATE
X.XXX	Y.XXX
X.XXX	Y.XXX
X.XXX	Y.XXX
GROUND	
X COORDINATE	Y COORDINATE
X.XXX	Y.XXX

NOTE

All coordinates are dimensioned from H-master 0 and identify typical point locations on the completed bare board.

4 OUTLINE DRAWING (OD)

At the request of the design engineer or manufacturing site, the locations of physical features that the design engineer deems critical shall be identified as such on the UA, if space permits. Critical features that cannot be clearly identified on the MD or UA shall be defined on a separate OD that shall be included as part of the 50-, 54-, or 70-class release package.

5 REVISIONS

The following sections contain part and document revision information.

5.1 PART REVISION

The 50-class part revision is the revision of the physical circuit data. Any changes to the physical circuit require a formal ECO to update the data base. The part revision level shown on the MD drawing must agree with the circuit board part revision. The 50-class part does not have to be released at Rev A1; the revision level is incremented per DEC STD 012-0 and release may occur at any revision level.

After the initial release of a PWB, a formal ECO is required to make any further changes. Pass numbers may be attached to a proposed new revision during design to allow engineering to evaluate as many passes of a change as necessary to correctly implement a *fix* without rewriting the ECO. The first pass number used is always *P1*. If further changes are necessary, the revision letter stays the same and the numeral increases. For example, P1 becomes P2. The pass number may remain on the PWB rather than going through another layout of the board to remove the number.

NOTE

The pass number is not a legitimate portion of the part identifier. It must be added as text and separated by a minimum of three character spaces from the part identifier.

5.2 DOCUMENT REVISION

The 50-class MD and its revision shall be listed on the appropriate 50-class DD. DEC STD 012-1 provides rules for the use of document revisions.

APPENDIX A REFERENCED DOCUMENTS

A.1 EL-Class Digital Documents

EL-Class Number	Document Title
EL-00012-00	<i>DEC STD 012-0 Part Identification Standard</i>
EL-00012-01	<i>DEC STD 012-1 Documentation Identification Conventions Including Mnemonic Codes</i>
EL-00013-01	<i>DEC STD 013-1 Standard Engineering Drawing Formats and Forms - General Purpose Drawing Sizes and Formats</i>
EL-00015-00	<i>DEC STD 015-0 Abbreviations and Units of Measurement</i>
EL-00024-00	<i>DEC STD 024-0 Top Document Requirements</i>
EL-00030-04	<i>DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements</i>
EL-00114-00	<i>DEC STD 114-0 Engineering Drawing Requirements - Industry Standards Adopted by Digital Engineering and Manufacturing Documentation Organizations</i>
EL-00114-01	<i>DEC STD 114-1 Engineering Drawing Requirements - Dimensioning and Tolerancing for Engineering Drawings</i>
EL-00128-00	<i>DEC STD 128-0 Security Classifications for Engineering Intellectual Property — Policy and Regulations</i>
EL-00140-00	<i>DEC STD 140-0 Documentation, Data, and Release Requirements for Printed-Wiring Boards, Modules, and Backplanes — Introduction</i>
EL-00140-02	<i>DEC STD 140-2 Documentation Requirements for 54-Class Modules and Backplanes</i>
EL-00176-00	<i>DEC STD 176-0 Printed-Wiring Board Acceptance Criteria</i>
EL-00185-00	<i>DEC STD 185-0 Documentation of Computer Media in the Engineering Documentation System</i>
EL-EN100-1A	<i>Engineering ECO Coordination Procedure</i>
EL-ENPCB-00	<i>PC Board Engineering Handbook — Special Feature Drawings</i>
EL-MFPCB-01	<i>PC Board Manufacturing Handbook - Volume 1</i>

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

A.2 Other Digital Documents

Document Number	Document Title
A-SP-1400000-GS-0	<i>Basic Specification for PC Boards and Material, Raw Stock and Finished Goods</i>

A.3 Ordering Information

Following are the sources for documents not available from Standards and Methods Control.

- Central Specification Control Systems
(NRO-5/M2), any Microfilm Reference File, or the SPOC System
- Reproduction Group
Sue Haywood, DTN: 223-2323
for hard copies of specification

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